LISTING OF SPECIFICATION AMENDMENTS

Please replace paragraph [0025] with the following amended paragraph:

[0025] Each control processor **104,106** runs all relevant routing protocol applications independently and produces the relevant tables required for packet forwarding. The forwarding information bases (FIB0 **108** and FIB1 **110**) derived from the respective control processors **104,106** are distributed to all STCs **112** regardless of their interface association. It should be noted that the respective FIBs are not necessarily identical, but are expected to contain the same reachability information. The next hop information will most likely not be the same, however. The packet forwarding engine **214** selects a set of FIBs to use at run-time, typically based on control processor association information. In accordance with an embodiment of the invention, ~~A~~ a FIB manager **230** receives FIB information ~~form~~ from the respective control processors **104,106** via busses **109,111** and writes the FIB information in the respective FIB0 **108** and FIB1 **110**. The FIB manager **230** is preferably programmed to write the MPLS FIBs so that the primary LSPs of FIB0 are created and maintained by control processor **104**, while the backup LSPs of FIB0 are created and maintained by control processor **106**. In FIB1, the primary LSPs are created and maintained by control processor **106**, while the backup LSPs are written by control processor **104**. Consequently, on transit core network traffic, diversely setup LSPs through the control processors **104,106** permit both line and equipment protection to be achieved in a single router **102** in accordance with the invention.

Please replace paragraph [0027] with the following amended paragraph:

[0027] The monitoring of a control processor to determine whether it is in-service is performed by monitoring critical software processes that it runs. The monitoring of an integrity of critical processes running on a control processor **104,106** is described with reference to FIGs. 3 and 4, and is performed by a heartbeat monitor **220**. Integrity of a control processor is defined as being "in-service" or "out-of-service". The heartbeat monitor **220** includes a tables of critical processes **304** that contain a list of selected processes **404** that run on the respective control processors **104,106**. The tables are referenced by a heartbeat inquiry generator **306**, which generates heartbeats **306A**, **306B**, . . . **306C** for respectively monitoring the integrity of process **404A**, **404B** and . . . **404C** running on the control processors **104,106**. The heartbeat monitor **220** sequentially generates and transmits the heartbeat inquiries **306A,306B,306C** to corresponding processes **404A,404B,404C** (FIG. 4). If each process **404A,404B,404C** returns a heartbeat response **308A,308B**, . . .**308C** within a predetermined period of time, the integrity of each process is declared "in-service". If any of the processes **404A,404B,404C** fails to return a heartbeat response **308A,308B,308C** within the predetermined period of time, the integrity of that process **404A,404B,404C** and the processor **104,106** that runs it is declared to be "out-of-service".

Please replace paragraph [0034] with the following amended paragraph:.

[0034] When a control processor **104** (for the purpose of the following discussion designated CPx) becomes unavailable due to a software crash, hardware fault, or for any other reason except a software upgrade (which is discussed below in some detail) all STCs **112** and the other control processor (designated CPy in this example) are notified. The packet forwarding engine **214** adjusts the control processor mastership of all affected interfaces to associate with

the remaining control processor CPy. The packet forwarding engine 214 adjusts all UNI Layer 1 and Layer 2 physical and logical port records to associate with the remaining control processor. the packet forwarding engine 214 also adjusts a control processor selection algorithm for any Layer 3 static (stub) interface (either NNI or UNI). CPy operates as if nothing has happened. The ~~Cpy~~ CPy still advertises its own routes, along with all the local routes of the CPx.